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Technical Report, ONR Program (N00014-01-1-0065)
Program period: October 1, 2000 to September 30, 2001

"Metamorphic HBTs: InP/InGaAs/InP devices grown on GaAs substrates"

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Abstract

This program supported the development of metamorphic heterojunction bipolar transistors (MHBTs). We accomplished this by growing an InP based HBT layer structure on GaAs substrates. InP metamorphic buffer layer was chosen in thermal point of view. Peak values of current-gain cutoff frequency (f_t = 207 GHz) and power-gain cutoff frequency (f_{max} = 140) were obtained from *rf* devices at bias conditions of V_{CE} = 1.5 Volts and $J_C = 4x10^5 A/cm^2$. These are the highest values reported for metamorphic HBTs.

Objectives

In recent years, research in high speed heterojunction bipolar transistors (HBTs) has been driven by circuit applications involving fiber IC chipsets at 40 Gb/sec, high frequency power amplifiers and new radar systems. HBTs with layers lattice-matched to InP substrates (InP HBTs) presently show the best high-frequency performance to realize these systems. These HBTs can have $In_{0.52}Al_{0.48}As$ or InP emitters, $In_{0.53}Ga_{0.47}As$ or $GaAs_{0.52}Sb_{0.48}$ base layers, and InP or $In_{0.53}Ga_{0.47}As$ collector layers. Their advanced performance results from the superior properties of In-based materials—including high electron mobility, large Γ-L energy separation, and low contact resistances. Unfortunately, InP substrates are small (10 cm) and much more expensive compared to GaAs substrates that are available in 15 cm diameters. Further, larger InP substrates are fragile and are readily broken during semiconductor manufacturing.

Extensive progress has been reported regarding metamorphic growth of InAlAs/InGaAs high mobility electron transistors (HEMTs) on GaAs substrates [1,2]. More recently, several groups [3,4] have reported InP-based HBTs grown on GaAs substrates, using InGaP or InGaAs metamorphic buffer layers. There the work focused on the physical quality of

[1] L.Edgar,N.I.Cameron,H.McLelland,M.C.Holland,M.R.S.Taylor,I.G.Thayne,C.R.Stanley,S.P.Beaumont, Electron Lett.,35,1114 (1999)

[2] S.Bollaert,Y.Cordier,V.Hoel,M.Zaknoune,H.Happy,S.Lepilliet,A.Cappy,IEEE Electron Device Lett.,20,123 (1999)

[3] H. Q. Zheng, K. Radhakrishnan, H. Wang, K. H. Yuan, S. F. Yoon, G. I. Ng, Appl. Phys. Lett., 77, 869 (2000)

[4] H. Hwang, J. Shieh, J. Chyi, Solid State Electron.,43,463 (1999)

the HBT epitaxial layers and the electrical performance of the device. Compared to HEMTs, HBTs have a larger active device area, the scales of integration are higher for HBT integrated circuits, and the devices typically operate at much higher power densities. Therefore, the crystal defect density *and* buffer layer thermal conductivity are both serious concerns that must be addressed in order for metamorphic HBTs to be practical.

Our goals were to develop high speed InP/InGaAs/InP and InAlAs/InGaAs heterojunction bipolar transistors (HBTs), grown and fabricated on GaAs substrates. We sought to demonstrate low leakage current HBT devices, even with metamorphic growth. Lastly we wanted to demonstrate that the thermal resistance of InP-related layers grown on GaAs can be made small, so that the high power densities associated with large integrated circuits and power amplifiers can be managed in the buffer layer and substrate.

Approach

Metamorphic HBTs were developed with emphasis placed on the characterization and the reduction of defects that are associated the leakage currents in metamorphic growth, and on reducing the thermal resistance of the metamorphic buffer layer. In order to accomplish this, several materials were tried, (InAlAs, AlGaAsSb, InP)—with InP chosen because of its high thermal conductivity.

Material property measurements of the metamorphic HBTs included surface roughness measurement by AFM, thermal conductivity, and MHBT junction leakage currents. Surface roughness and thermal conductivity data are shown in table 1.

Material	Thermal conductivity (W/mK)	RMS roughness (nm)
Metamorphic AlGaAsSb	8.4	4.0
Metamorphic InAlAs	10.5	11.7
Metamorphic InP	16.1	9.5
GaAs bulk	44	
InP bulk	68	

Table 1: Surface roughness and thermal conductivity data of three metamorphic buffer layers

Buffer layer thermal conductivities were determined by measuring the thermal impedance of 1 μm x 100 μm Pt conductors of 50 nm thickness [5]. These conductors were deposited on the buffer layers after removing the HBT layer structure. The InP buffer layer shows the highest measured thermal conductivity, although it is much smaller than known for bulk InP. This is most probably due to the poor crystal quality of the metamorphic layer.

[5] A. W. Jackson, J. P. Ibbetson, A. C. Gossard, U. K. Mishra, Appl. Phys. Lett., 74, 2325 (1999)

In order to determine the influence of the metamorphic buffer layer's thermal conductivity on device temperature, the expected HBT collector junction temperature was calculated by solving the Laplace heat flow equation in 3 dimensions. A 45 μm device-device separation was assumed for 30 HBTs—typical of smaller HBT integrated circuits. The assumed HBT emitter size was 8×0.5 μm^2 and the operating power density was $2 \cdot 10^5$ W/cm^2. A 1.5 μm thick metamorphic buffer layer on a GaAs substrate was assumed. The heat flow simulations in figure 1 indicate that the HBT junction temperature is strongly influenced by the thermal conductivity of the metamorphic layer, and that the measured differences in thermal conductivity between AlGaAsSb (8.4 W/mK), InAlAs (10.5 W/mK), and InP (16.1 W/mK) buffer layers will have a considerable impact on the HBT operating temperature.

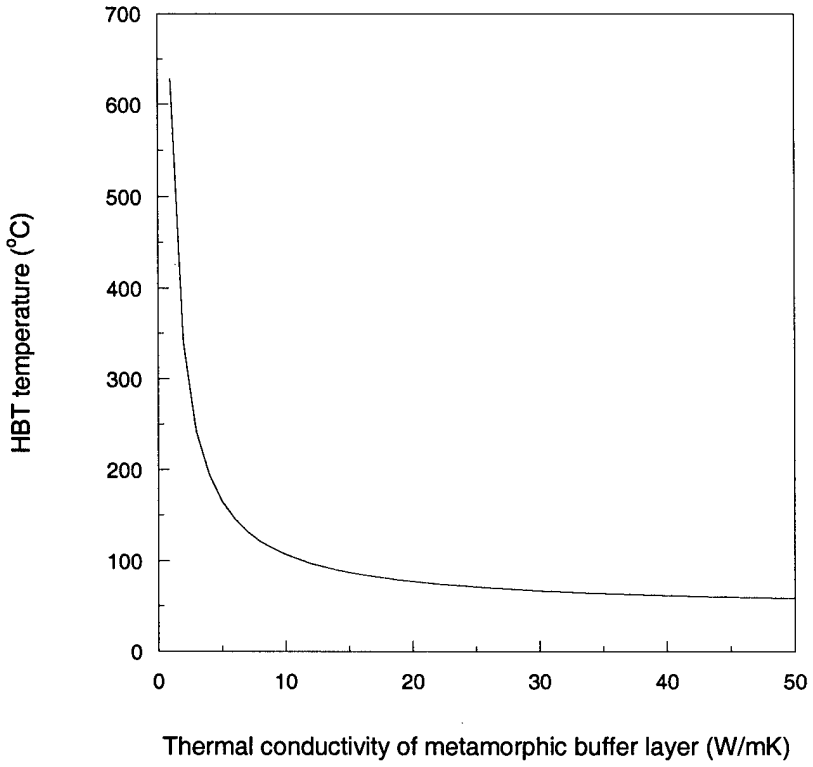

Fig 1. Dependence of MHBT operating temperature on the thermal conductivity of the metamorphic layer. A metamorphic buffer layer thickness of 1.5 μm is assumed.

The expected HBT junction temperature was calculated to be 128°C, 112°C, and 89°C for AlGaAsSb, InAlAs, and InP buffer layers for the above device dimensions and power densities. This should be compared to a computed 65°C junction temperature which would result for a buffer layer of negligible thickness. Using the InP-based HBT reliability data[6], the calculated HBT life-time is reduced by two orders of magnitude

[6] K.Kiziloglu, S. Thomas, F.Williams, B.M.Paine, IEEE Conference on Indium Phosphide and Related Materials, May, Williamsburg, VA, 294 (2000)

when the junction temperature is increased from 100°C to 150°C. The lifetimes of HBTs operating at a $2 \cdot 10^5$ W/cm^2 power density using InAlAs and AlGaAsSb buffer layers would approximately be 20:1 and 100:1 shorter than that of an HBT using an InP buffer layer. As HBT device and circuit speed is increased, the HBT operating power density must be increased beyond $2 \cdot 10^5$ W/cm^2. Improvements in the thermal conductivity of the metamorphic layer are thus extremely important in future device design. Computed device junction temperatures as a function power density are shown in figure 2.

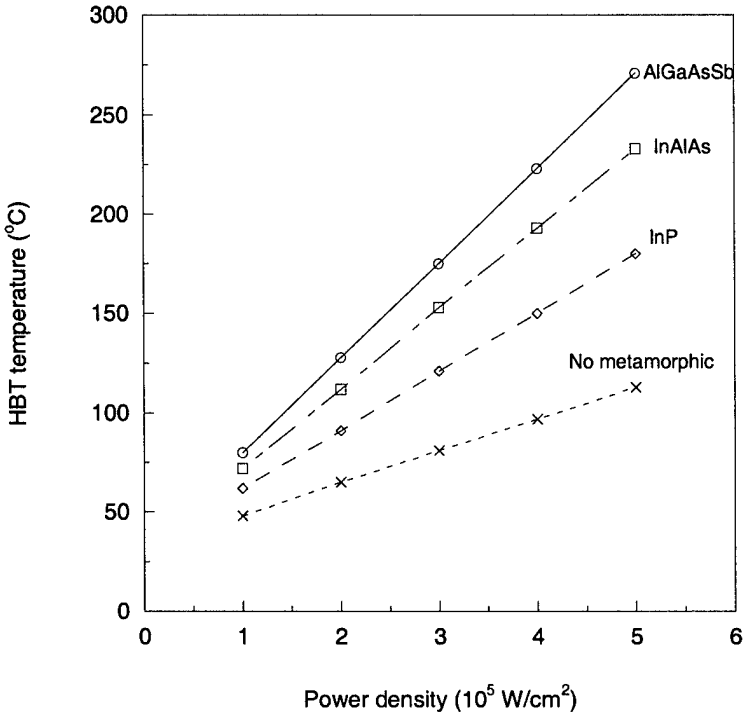

Fig 2. Dependence of HBT device temperature with operating power density

Accomplishments

The devices fabricated employed an MBE epitaxial double-hetero layer structure with an InP emitter, 400 Å graded $In_{0.53}GaAs$ highly doped base layer (Be: $4.0 \cdot 10^{19}$cm^{-3}), a 100 Å InGaAs setback layer, a 240 Å CSL base-collector grade and a 1630 Å InP collector layer, resulting in a total collector depletion layer thickness of 2kÅ. HBTs were fabricated in a narrow triple-mesa process using optical projection lithography and selective wet chemical etching. The use of narrow base-emitter and collector-base junctions reduces both the base resistance and the collector-base capacitance, and hence the charging times associated with these parasitics. While the emitter contact metal is 0.7×8 μm^2, the emitter semiconductor is laterally undercut during the InP HCl-based etch. Because of this undercut, the physical base-emitter junction is 0.4×7.5 μm^2. The collector-base capacitance is reduced by employing self-aligned, narrow base ohmic contacts of 0.25 μm width on both sides of the emitter stripe— producing a small 1.2 μm × 11 μm collector-

base junction area. After the deposition of base metal, the base and collector semiconductor are etched, exposing the device subcollector. Collector contacts are deposited and then devices are isolated by etching the remaining HBT semiconductor to the metamorphic layer. Polyimide is then deposited, cured, and etched for passivation and mesa planarization prior to interconnect deposition.

Figure 3 shows the common emitter characteristics, with a measured current density from 0 to $4 \cdot 10^5$ A/cm^2. The measured DC current gain is approximately 76, with a common-emitter open-circuit breakdown voltage BV_{CEO} at low current densities greater than 6 V, while $V_{CE,\,Sat} < 0.8$ V at a current density of $4 \cdot 10^5$ A/cm^2. The measured sheet resistance of the metamorphic InP buffer layer is roughly 150 MΩ / square. The base sheet resistance is 1020 Ω / square —measured after the emitter mesa etch (which removed the upper 100 Å of the base layer) and base metal deposition. The corresponding hole mobility is 51 cm^2 / V·sec — 10% lower than we observe for similar lattice-matched DHBT growths.

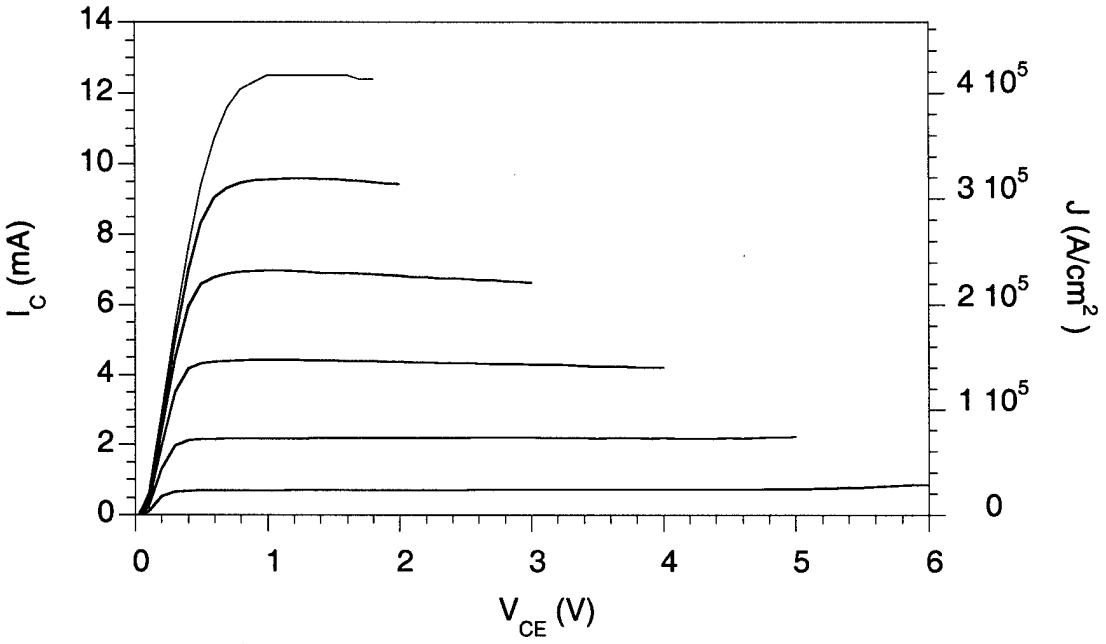

Fig 3. DC characteristics for common emitter MHBT— 0.4 × 7.5 μm^2 emitter area. The base current steps are 40 μA.

Figure 4 shows the HBT Gummel [log(I_C, I_B) vs V_{CE}] characteristics, indicating a collector current ideality factor of 1.1 and a base current ideality factor of 2.2. The characteristics are measured with as non-zero (0.3 V) reverse bias applied to the collector-base junction, so that base-collector junction leakage, if present, will be observed. For comparison, figure 4 also shows the Gummel characteristics of a large-area HBT—60 × 60 μm^2 base-emitter and 100 × 130 μm^2 base-collector junctions fabricated from the same epitaxial material. Despite the large collector-base junction area, the Gummel characteristics indicate that I_{cbo} of the large-area HBT is below 0.1 μA, signifying a collector-base leakage current per unit junction area below 10^{-3} A/cm^2.

The small-area HBTs were fabricated on a mask set designed with microwave on-wafer probe cal standards using the line-reflect-line method in a 50 Ω coplanar waveguide (CPW) environment. The line length between the probe pad and device terminal is 230 μm. The leakage currents observed at low V_{BE} in figure 4 for the small-area HBT are dominated by those associated with conduction through the buffer layer between these long interconnects. And while HBTs are minority-carrier devices, and defect-induced leakage currents resulting from metamorphic growth are potential concerns, high DC current gains and low $< 10^{-3}$ A/cm^2 base-collector leakage are nevertheless observed .

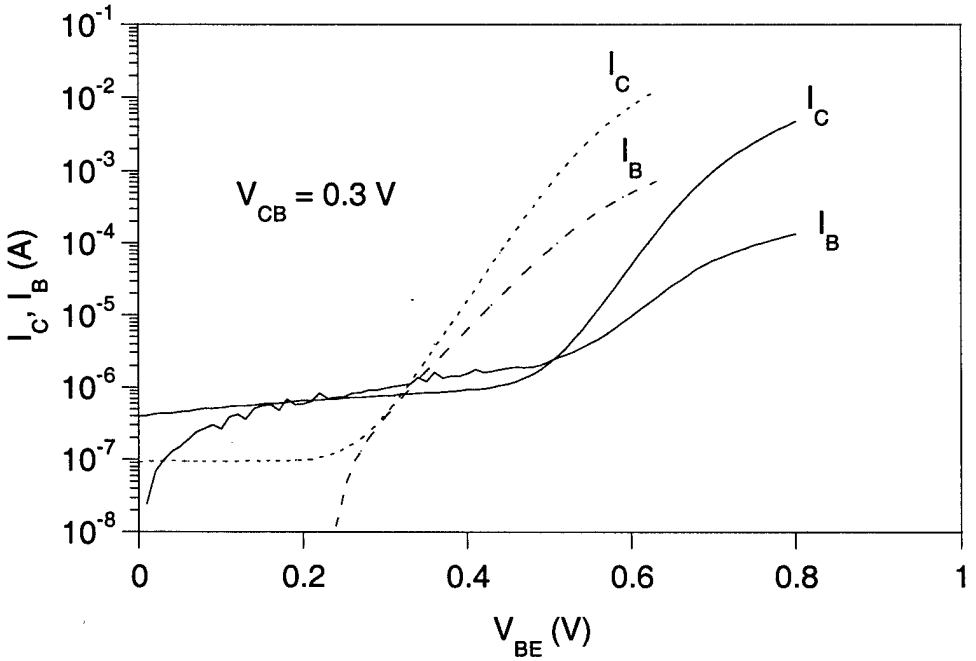

Fig 4. Metamorphic HBT Gummel characteristics—
***Device A* (solid lines) represents a 0.4 × 7.5 μm^2 base-emitter junction and a 1.2 × 11 μm^2 base-collector junction,**
***Device B* (dashed lines) represents a 60 × 60 μm^2 base-emitter junction and a 100 × 130 μm^2 base-collector junction.**

Figure 5 shows the short circuit current gain (h_{21}) and unilateral power gain (U) of the small-area HBTs, computed from the measured 45 MHz to 45 GHz S-parameters. A current-gain cutoff frequency f_τ = 207 GHz and power-gain cutoff frequency f_{max} = 140 GHz were measured at I_C = 12.0 mA ($J_C = 4 \cdot 10^5 A/cm^2$) and V_{CE} = 1.5 V, as determined by a -20 dB/decade extrapolation. These are the highest values reported for metamorphic HBTs. Figure 6, shows the variation of f_τ and f_{max} with collector current density, as measured at V_{CE} = 0.7 V and V_{CE} = 1.5 V. The observed decrease in f_τ at very high current densities ($2.5 \cdot 10^5$ A/cm^2 at V_{CE} = 0.7 V, 4.5×10^5 A/cm^2 at V_{CE} = 1.5 V) is due to the Kirk effect.

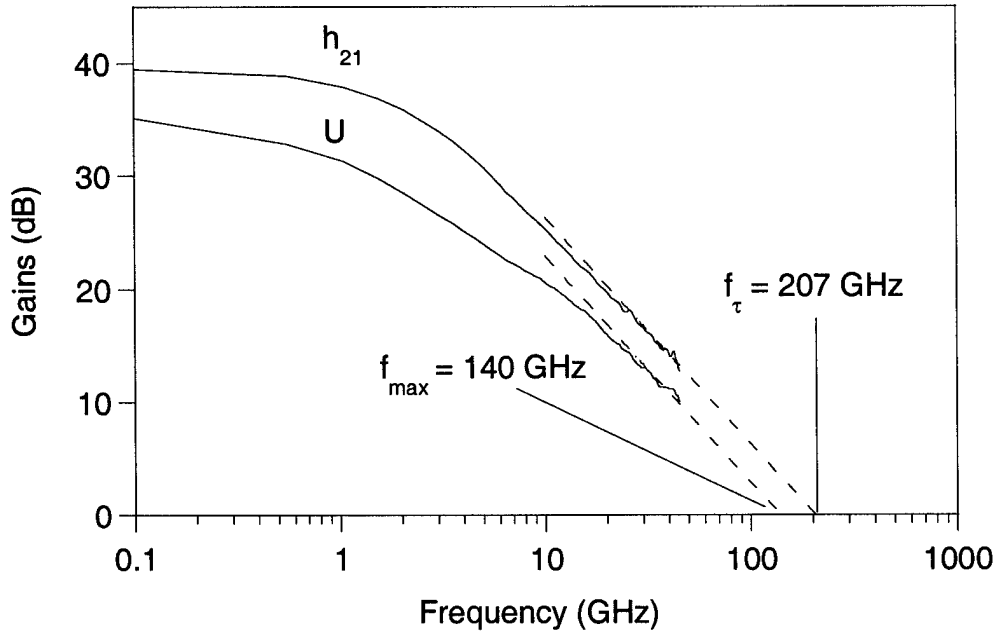

Fig 5. Short-circuit current gain, h_{21} and Mason's unilateral power gain, U for an MHBT. Device dimensions: 0.4 × 7.5 μm^2 base-emitter junction and a 1.2 × 11 μm^2 base-collector junction. DC bias conditions: I_C = 12.0 mA, J_C = 4 mA / um^2, and V_{CE} = 1.5 V

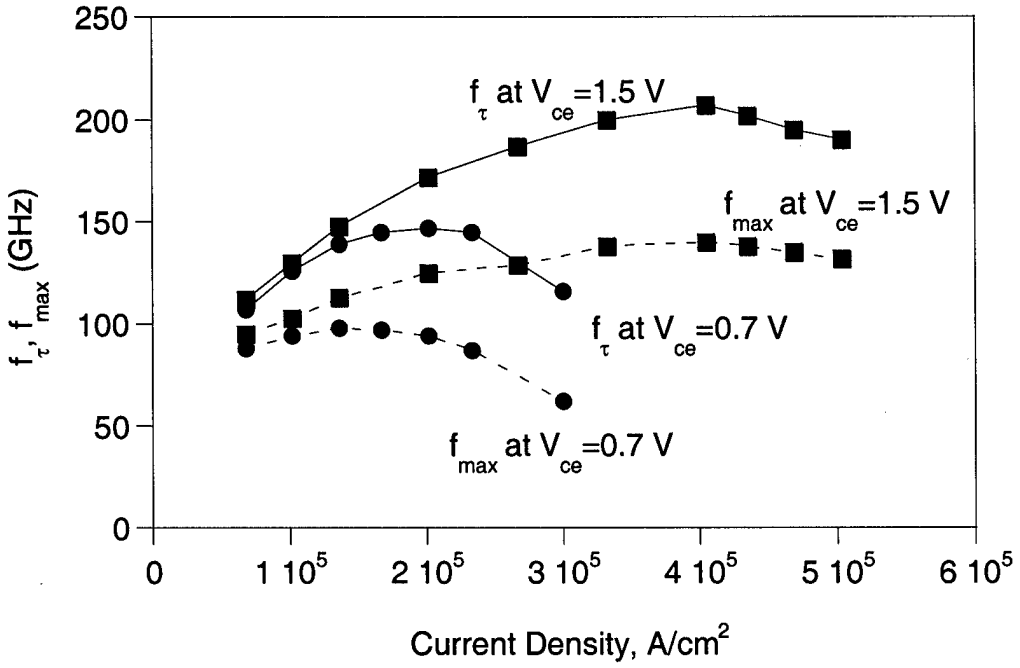

Fig 6. Measured current-gain cutoff frequency f_t, and power-gain cutoff frequency f_{max} vs. current density J_C at V_{CE} = 0.7 Volts and V_{CE} = 1.5 Volts.

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YoungMin Kim, PhD. 1997
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1	2002	Y.M.Kim, M.J.W.Rodwell, A.C.Gossard, Thermal characteristics of InP,InAlAs, and AlGaAsSb metamorphic buffer layers used in InAlAs/InGaAs heterojunction bipolar transistors grown on GaAs substrates, ,	Journal of Electronic Materials, Vol.31, pp.196-199, 2002	Journal Paper
2	2001	Y.M. Kim, M. Dahlstrom, S. Lee, M.J.W. Rodwell, A.C. Gossard. $InP/In_{0.53}Ga_{0.47}As/InP$ Double Heterojunction Bipolar Transistors on GaAs Substrate Using InP Metamorphic Buffer Layer	. International Semiconductor Device Research Symposium December 5-7, 2001Washington, D.C. p 638-639	Conference Paper
3.	2002	Y.M. Kim, M. Dahlstrom, S. Lee, M.J.W. Rodwell, A.C. Gossard, "$InP/In_{0.53}Ga_{0.47}As/InP$ Double Heterojunction Bipolar Transistors on GaAs Substrate Using InP Metamorphic Buffer Layer."	Solid State Electronics, Vol.46, pp.1541-1544, 2001. Journal Paper	Journal Paper
4	2002	Y.M. Kim, M. Dahlstrom, S. Lee, M.J.W. Rodwell, A.C. Gossard, High-Performance $InP/In_{0.53}Ga_{0.47}As/InP$ Double Heterojunction Bipolar Transistors on GaAs Substrates.	IEEE Electron Device Letters Vol.23, No.6, pp. 297-299, 2002	Journal Paper